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June 13, 2003

VIA FACSIMILE

To: Examiner Erik J. Kielin
Group Art Unit No. 2813
U.S.P.T.O.

Facsimile No.: (703) 872-9318

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From: Sean M. McGinn

Facsimile No.: (703) 761-2375 JUN 13 2003

Re: Enclosed § 1.111 Amendment
U.S. Patent Application Serial No. 09/902,483
Our Ref: YOR.129CIP

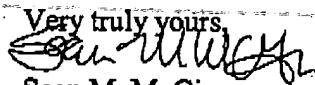
TECHNOLOGY CENTER 2800

Dear Examiner Kielin:

Enclosed is an Amendment, responsive to the March 13, 2003 Office Action, which should place the above-referenced case in condition for allowance.

Thank you in advance for your kind consideration on this case.

Very truly yours,


Sean M. McGinn

SMM/sm
Enclosure

Total No. of Pages Transmitted: 17

09/902,483
YOR919990408CIP

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Cabral et al.

Serial No.: 09/902,483

Group Art Unit: 2813

Filed: July 11, 2001

Examiner: Erik Kielin

For: SELF-ALIGNED SILICIDE (SALICIDE) PROCESS FOR LOW RESISTIVITY
CONTACTS TO THIN FILM SILICON-ON-INSULATOR AND BULK MOSFETS
AND FOR SHALLOW JUNCTIONS

Honorable Commissioner of Patents
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

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In response to the Office Action dated March 13, 2003, please amend the above-
identified application as follows:

JUN 13 2003

TECHNOLOGY CENTER 2800

IN THE CLAIMS:

5. (Amended) The method of claim 4, wherein said depositing of said metal containing silicon
comprises performing a blanket deposition, wherein said metal comprises one of Co and Ti.

7. (Amended) The method of claim 6, wherein said blanket deposition is followed by a TiN cap
deposition for preventing oxidation during a subsequent anneal processing.

8. (Amended) The method of claim 4, wherein said reacting of said metal containing silicon or
said alloy comprises performing a first rapid thermal anneal (RTA) to form a metal-silicon phase,
such that the deposited metal containing silicon with the underlying bulk silicon substrate,